YM3411

Surround Processor (SP)

■ Introduction

The YM3411, a 16-pin DIP C-MOS LSI, permits to implement digital surround sound capabilities realized by Yamaha's digital audio technology.

As the LSI includes A/D and D/A converters, you can easily implement digital surround functions without any additional analog devices.

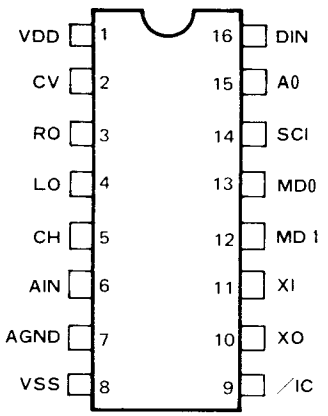
It has four delay lines each of which may be set for the maximum delay time of 30.24 msec, and outputs are two channels each of which is produced in each pair of delay channels added up digitally. So, the range of application is wide.

■ Features

- Three kinds of surround mode are possible as preset modes without the use of any microcomputers.
- With a use of microcomputer, it is possible to set the four delay lines at different delay times and different volumes and to define parameters of a primary IIR digital low-pass filter.
- The internal signal format is of 14-bit floating point numbers.
- The built-in A/D and D/A converters are of floating type with high linearity.
- The built-in reference voltage generator for A/D Converter permits an easy interface with analog circuits.
- The A/D converter operates at the sampling frequency of 49.7 kHz. And its output signal data passes a 1/2 undersampling digital filter, so that high cost external input low-pass filter is not needed.
- The D/A converter operates at the sampling frequency of 99.4 kHz, following a built-in quadruple oversampling digital filter, so that high cost external output low-pass filter is not needed.

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■ Package pin arrangement



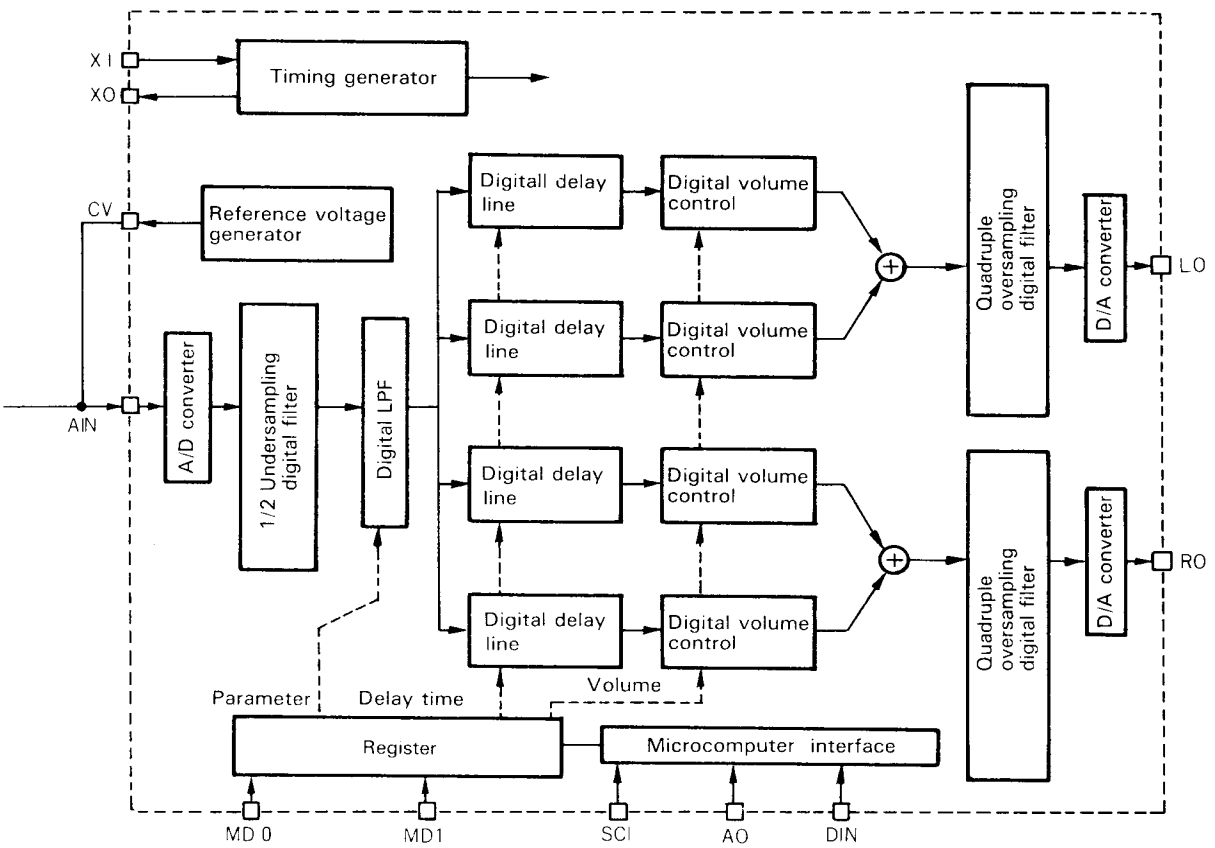
TOP VIEW

■ Pin assignments

Pin No.	Symbol	I/O	Description
1	VDD	—	+5V power
2	CV	O	+2.5V reference voltage (output) for A/D converter
3	RO	O	R-channel output (analog)
4	LO	O	L-channel output (analog)
5	CH	O	Connects to external sample-hold capacitor
6	AIN	I	Analog signal input (with CV as reference voltage)
7	AGND	—	Ground of A/D and D/A converters (must be connected to VSS at outside)
8	VSS	—	System ground of digital circuits
9	/IC	*I	Reset terminal
10	XO	O	Connects to a quartz crystal oscillator
11	XI	I	(Input of external clock signal, if used)
12	MD1	*I	Mode setting terminal
13	MD0	*I	
14	SCI	I	Clock input for data shift when a microcomputer is used
15	A0	I	Input of address/data identifying signal when a microcomputer is used
16	DIN	I	Data input when a microcomputer is used

* indicates that a pullup resistor is built in.

■ Block diagram



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■ System block diagram

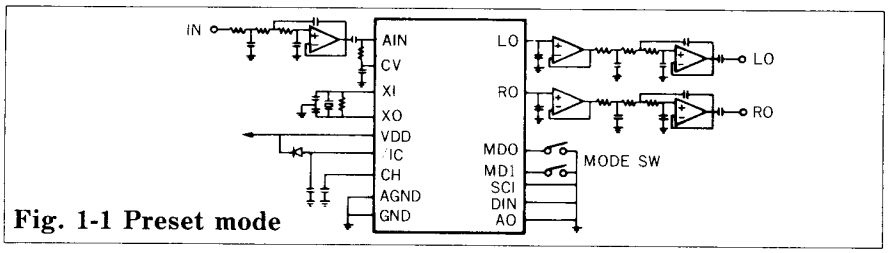


Fig. 1-1 Preset mode

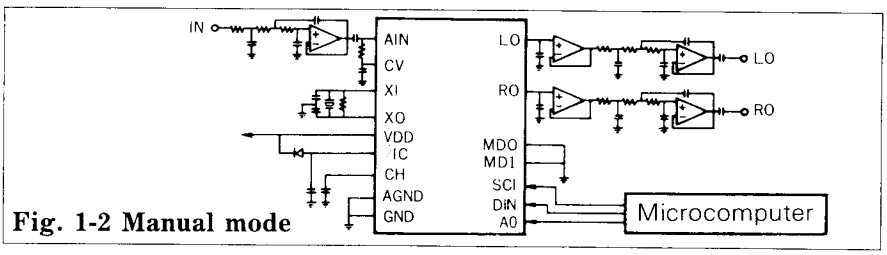


Fig. 1-2 Manual mode

■ Description

As shown in a block diagram below, analog input signal coming to the terminal AIN enters a 14-bit floating A/D converter, which samples the input signal at the rate of 49.8 kHz and converts it to digital signal format of 14-bit floating point numbers. The output of the A/D converter enters a 1/2 undersampling digital filter. This decays 12.4 ~ 37.3 kHz by more than 25 dB to eliminate the external LPF at the input circuit. Its sampling rate is 24.9 kHz. The output of the 1/2 undersampling digital filter parameters enters a primary IIR LPF. (The cut-off frequency of this filter may be controlled with the parameters set in the registers A0, A1 and B1 from a microcomputer connected.)

The digital delay unit consisting of RAM has four output taps which can be switched by the set in of the registers DL0, DL1, DR0 and DR1.

The output signals come from the taps to digital volume units. In these units, volume registers GL0, GL1 and GR1 decay the signal levels digitally. Then adders produce L0+L1 and R0+R1. These outputs enter quadruple oversampling digital filters individually. This oversampling filter decays the input signal by about 25 dB in its cutoff region to reduce loop-back noises which would appear after D/A conversion. This eliminates the external LPF at the output circuit. The sampling rate of this filter is 99.4 kHz.

To perform such digital processing, the LSI executes ROM programs.

In a preset mode, parameters will be provided as ROM data, so the microcomputer is not necessary.

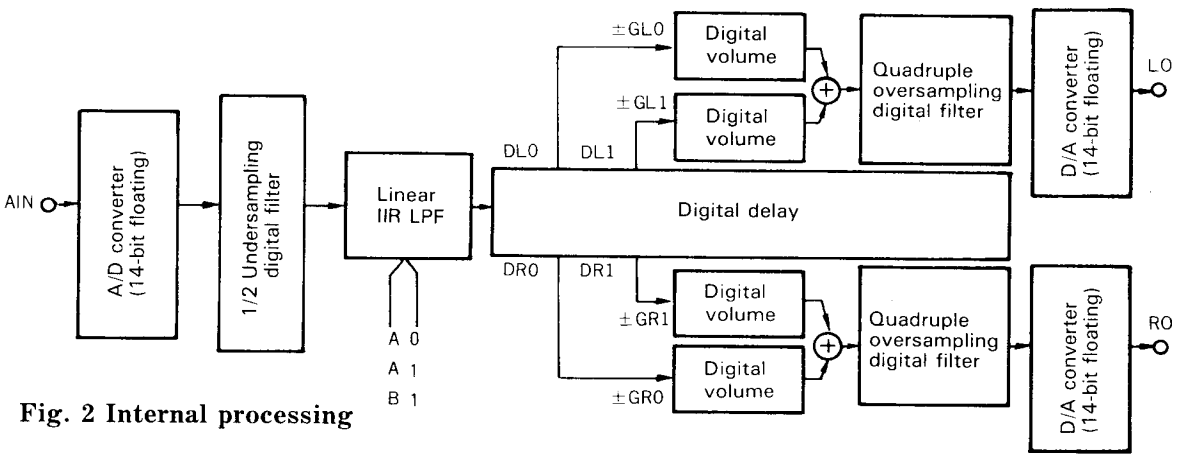


Fig. 2 Internal processing

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■ Setting preset modes and characteristics

- **[Hall Surround]** (MD0="L", MD1="H")
  Hall surround signals LO and RO is produced from level difference between long and intermediate delays. When the L+R signal (monaural) is come to the AIN terminal, Hall Surround effect will occur.
- **[Simulated Stereo]** (MD0="H", MD1="L")
  Simulated stereo signals LO and RO is produced from a monaural input signal by inverting phase of long delay with high level and short delay with low level. The input is L+R and the outputs LO and RO come out through the front speakers.
- **[Dolby Surround]** (MD0="H", MD1="H")
  The L—R signal will come to the AIN terminal. The output LO or RO will be supplied to an external Dolby decoder connected. As LO and RO have different delay times, there are choices of two Dolby modes by switching the outputs LO and RO.

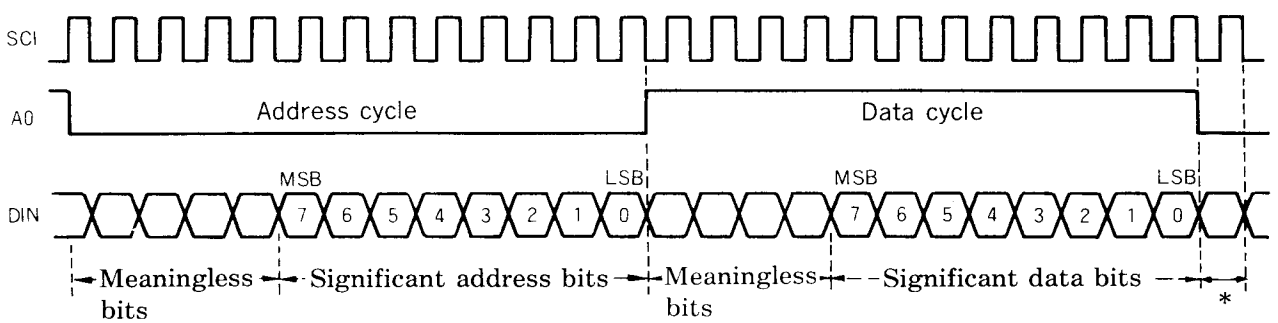
■ Register address map

The LSI operates in manual mode when MD0="L" and MD1="L". To use the LSI in manual mode, data must be set in the registers from a microcomputer as explained below.

Address (HEX)	Data/registers								Parameter
	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
0 0	X	X	±	DL 0					Lch 0 polarity/delay time
0 1	X	X	±	DL 1					Lch 1 polarity/delay time
0 2	X	X	±	DR 0					Rch 0 polarity/delay time
0 3	X	X	±	DR 1					Rch 1 polarity/delay time
0 4	GL 1				GL 0				L-channel volume level
0 5	GR 1				GR 0				R-channel volume level
0 6	X	X	X	X	A 0 (High order)				LPF parameter A 0
0 7	A 0 (Low order)								
0 8	X	X	X	X	A 1 (High order)				LPF parameter A 1
0 9	A 1 (Low order)								
0 A	X	X	X	X	B 1 (High order)				LPF parameter B 1
0 B	B 1 (Low order)								

Notes * : X means "Don't care".
* : Data may be written in the registers whatever values MD0 and MD1 are set at. You have to fill all the registers with data before setting MD0="L" and MD1="L".
* : Mute the outputs while writing in LPF parameters : otherwise unusual sounds might be produced.

- **Microcomputer interface**



* After the fall of AO in the last data, send out SCI for one clock period or more.

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■ Register data

- **Setting output polarity** ($H00 ~ $H03 D5 : ±)
  When D5="1", the output signal is in phase with the input signal.
  When D5="0", the output signal is in opposite phase with the input signal.
- **Setting delay time** ($H00 ~ $H03 : DL0, DL1, DR0, DR1)

Delay time (mS)	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	0
1.44	0	0	0	0	1
2.88	0	0	0	1	0
4.32	0	0	0	1	1
5.76	0	0	1	0	0
7.20	0	0	1	0	1
8.64	0	0	1	1	0
10.08	0	0	1	1	1
11.52	0	1	0	0	0
12.96	0	1	0	0	1
14.40	0	1	0	1	0

Delay time (mS)	D 4	D 3	D 2	D 1	D 0
15.84	0	1	0	1	1
17.68	0	1	1	0	0
18.72	0	1	1	0	1
20.16	0	1	1	1	0
21.60	0	1	1	1	1
23.04	1	0	0	0	0
24.48	1	0	0	0	1
25.92	1	0	0	1	0
27.36	1	0	0	1	1
28.80	1	0	1	0	0
30.24	1	0	1	0	1

Note : If you set a delay time longer than 30.24 msec (beyond "10101") ; unusual sound would be produced.

- **Setting volume level** ($H04, $H05 : GL0, GL1, GR0, GR1)

Setting volume level		D 3	D 2	D 1	D 0	GL 0, GR 0
(Decimal)	(dB)	D 7	D 6	D 5	D 4	GL 1, GR 1
0.875	−1.16	1	1	1	1	
0.75	−2.50	1	1	1	0	
0.625	−4.08	1	1	0	1	
0.5	−6.00	1	1	0	0	
0.4375	−7.18	1	0	1	1	
0.375	−8.52	1	0	1	0	
0.3125	−10.1	1	0	0	1	
0.25	−12.0	1	0	0	0	
0.21875	−13.2	0	1	1	1	
0.1875	−14.5	0	1	1	0	
0.15625	−16.1	0	1	0	1	
0.125	−18.1	0	1	0	0	
0.109375	−19.2	0	0	1	1	
0.09375	−20.6	0	0	1	0	
0.078125	−22.1	0	0	0	1	
0		0	0	0	0	

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- **Setting LPF parameters** ($H04, $H0B : A0, A1, B1)

Register	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
A0	Address $H06								Address $H07							
A1	Address $H08								Address $H09							
B1	Address $H0A								Address $H0B							
bit	X	X	X	X	11	10	09	08	07	06	05	04	03	02	01	00
Parameter					SIN	Exponent			Mantissa							

△ Decimal point position

SIN is a sign bit; "1" for plus and "0" for minus.
The exponent means that, when its value is EX, the parameter value is given by the mantissa multiplied by the EXth power of 2.

bit D10	D09	D08	D07	EX	Exth power of 2 (decimal)
0	0	0	0	−0	1
1	1	1	1	−1	0. 5
1	1	1	0	−2	0. 2 5
1	1	0	1	−3	0. 1 2 5
1	1	0	0	−4	0. 0 6 2 5
1	0	1	1	−5	0. 0 3 1 2 5
1	0	1	0	−6	0. 0 1 5 6 2 5
1	0	0	1	−7	0. 0 0 7 8 1 2 5
1	0	0	0	−8	0. 0 0 3 9 0 6 2 5

The mantissa is bits 06—00 with the decimal point existing between bit 06 and 05. The mantissa must be normalized in such a manner that the content of bit 06 is 1, unless the value is 0.

[Examples of parameters]

f c	$H06	$H07	$H08	$H09	$H0A	$H0B
3 KHz	00001111	01001001	00001111	01001001	00001111	01101110
4 KHz	00001111	01011011	00001111	01011011	00001111	01001010
5 KHz	00001111	01101100	00001111	01101100	00001110	11010000
6 KHz	00001111	01111100	00001111	01111100	00001101	11000000
7 KHz	00001111	11000110	00001111	11000110	00000110	01100000
8 KHz	00001111	11001110	00001111	11001110	00000110	11110000
Flat	00001000	01000000	00000000	00000000	00000000	00000000

■ Electrical characteristics

- **1. Absolute maximum ratings** (VSS=0.0V)

Parameter	Symbol	Rating	Unit
Terminal voltage	VDD—VSS	−0.3 ~ 7.0	V
Operating temperature	TOP	0 ~ 70	°C
Storge temperature	Tstg	−50 ~ 125	°C

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- **2. Recommended operating conditions** (VSS=0.0V, TOP=0~70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	VDD	4.75	5.00	5.25	V
	VSS, AGND	0	0	0	V

- **3. DC characteristics** (VDD=4.75~5.25V, TOP=0~70 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low-level input voltage	VIL		−0.3		0.8	V
High-level input voltage	VIH	Except XI	2.0		VDD	V
High-level input voltage	VIH	XI	4.0		VDD	V
Low-level output voltage	VOL	XO : IOL=0.2 mA	−0.3		0.4	V
High-level output voltage	VOH	XO : IOH=0.4 mA	4.0			V
Input current leak	ILK	VI=5V			10	μA
Supply current	IDD			20.0	30.0	mA
Input capacitance	CI	f=1 MHz			10	pF
Output capacitance	CO				10	pF
Pullup resistance	RPU	/IC, MD0, MD1	50		400	KΩ

- **4. AC characteristics** (VDD=4.75~5.25V, TOP=0~70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
XI clock input frequency	fc	1.8	3.58	4.5	MHz
XI clock input duty		40	50	60	%
XI clock rise time				50	nS
XI clock fall time				50	nS
SCI clock input frequency				fc × 1/4	MHz
SCI clock on time		600			nS
SCI clock rise time				200	nS
SCI clock fall time				200	nS

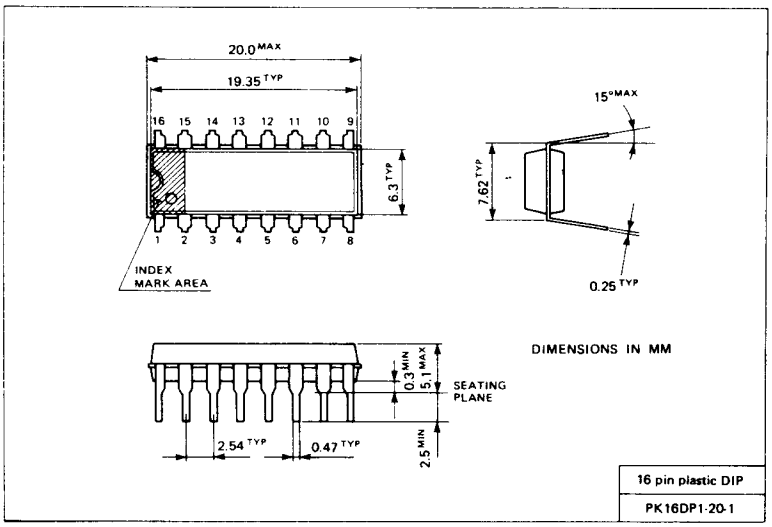
- **5. Analog characteristics** (VDD=5.0V, TOP=0~70 °C)

Parameter	Symbol	Condition	TYP.	MAX.	Unit
Analog input voltage	VIA	AIN		4.5	VP−P
Analog output voltage (*1)	VOA	RO, LO		4.5	VP−P
DC offset voltage	CV		2.5		V
Total harmonic distortion (*2)	THD	Output voltage	0.5	0.6	%
		−10 dB	0.55	0.65	%
		−20 dB	0.6	0.7	%
		−30 dB	1.3	1.7	%
Signal-to-noise ratio (*3)	S/N	S=max.	80	75	dB

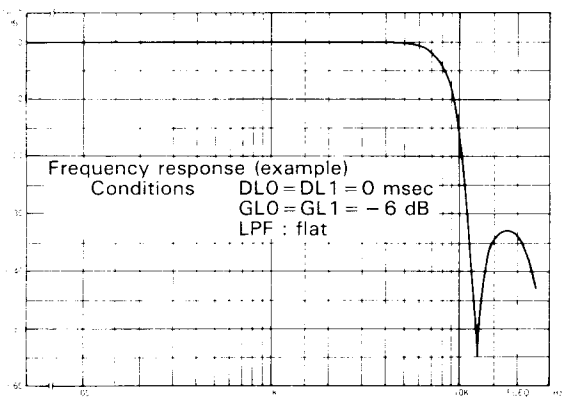
Notes *1 : External resistance RL=470 kΩ
*2 : The total harmonic distortion here is THD+noise.
fc=3.58 MHz, input signal frequency=1 kHz,internal LPF=flat (through), with external filter (cutoff frequency 10 kHz, 18 db/oct) at output
*3 : fc=3.58 MHz, internal LPF=flat (through),
S : 1-kHz input for 4.5 Vp-p output
N : under zero signal, with external filter (cutoff frequency 10 kHz, 18 db/oct) at output

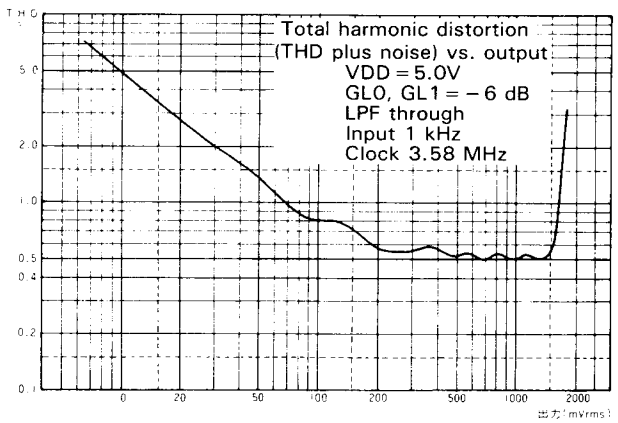
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■ External views



■ Characteristics (reference data)





Notes : ● The specifications are subject to changes for improvement without prior notice.
● The standard clock frequency of XI is 3.58 MHz in this catalog.

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